UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,068	04/19/2001	Wilhelm E. Haller	DE920000008US1	8778

7590 10/22/2003

Blanche E. Schiller, Esq.
HESLIN & ROTHENBERG, P.C.
5 Columbia Circle
Albany, NY 12203

EXAMINER	
PATEL, HARESH N	

ART UNIT	PAPER NUMBER
2126	5

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,068	HALLER ET AL.	
	Examiner	Art Unit	
	Haresh Patel	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) 6-11 is/are objected to.

8)☒ Claim(s) 1-14 are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04/19/01 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-14 are presented for examination.

Priority

2. Applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) or (f), is acknowledged.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "An Improved system and method to optimize usage of the Instruction Window Buffers (IWB) by adding a simple combinatorial circuit in a parallel processing multiprocessor environment".

4. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The abstract of the disclosure is objected to because it does not contain key terms of the invention, like, Instruction Window Buffer, multi-processor, parallel processing, etc. Also the abstract must not contain "preferably" key word. Correction is required. See MPEP § 608.01(b).

Information Disclosure Statement

5. Applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the examiner has determined is reasonably necessary to the examination of this application.

In response to this requirement, please provide the title, citation and copy of each publication that is a source used for the description of the prior art in the disclosure. For each publication, please provide a concise explanation of that publication's contribution to the description of the prior art.

This Office action has an attached requirement for information under 37 CFR 1.105. A complete reply to this Office action must include a complete reply to the attached requirement for information. The time period for reply to the attached requirement coincides with the time period for reply to this Office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 6 is rejected under undue breadth, 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 6-8 and 9-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claims 6-8 recites the limitation "Buffer storage device". There is insufficient antecedent basis for this limitation in the claim.

9. Claims 9 and 10 recites the limitation "sub-unit". There is insufficient antecedent basis for this limitation in the claim.

10. Claim 11 recites the limitation "microprocessor device". There is insufficient antecedent basis for this limitation in the claim.

11. It is not clear whether claims 9-11 are dependent claims of claim 6. However, Examiner considers claims 9-11 as dependent claims for the examination purpose.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Soell et. al. 5,923,900 (Hereinafter Soell).

14. As per claims 1, 6 and 12, Soell teaches the following:

a buffer storage device having a plurality of n entries, the entries being subject of at least one process to work on, and comprising,

a computer system having a microprocessor device, said microprocessor device having at least one sub-unit, said at least one sub-unit having one or more storage devices, at least one storage device of said one or more storage devices having a plurality of n entries, the entries being subject of at least one process to work on, and said at least one storage device comprising:

a method for operating a buffer memory, the buffer having a plurality of entries, the entries being subject of at least one process to work on, said method comprising,

generating for each of said entries (e.g., real entry positions in the buffer, abstract) validation information which is evaluable for the status of an entry relative to its further processing (e.g., each entry which fulfills the given condition blocks a certain number of adjacent entries, including said virtual entries. One entry will remain which is not blocked, and

which also fulfills the given condition. This entry is the entry with sequential priority, abstract) by said at least one process (e.g., The invention relates to a circular buffer containing a sequence of entries, and in particular to determining a sequential priority among entries which both fulfill a given condition and are contained in said sequence. This problem is not straightforward, because said sequence of entries may wrap-around in said circular buffer, which means that said sequence of entries extends beyond the last entry position of the buffer. According to the invention, first, a number of virtual entry positions, which is at least equal to the number of real entry positions in the buffer, is added to the non-occupied part of the buffer. In a second step, each entry which fulfills the given condition blocks a certain number of adjacent entries, including said virtual entries. One entry will remain which is not blocked, and which also fulfills the given condition. This entry is the entry with sequential priority, abstract).

15. As per claims 2, 3, 5, 7-8 and 13 and 14, Soell teaches the following:

said validation information is specific for each of a plurality of processes and indicating if a respective entry can be subjected to a respective process, or not (e.g., each of said predetermined entries of said subset of predetermined entries, at least (n-1) adjacent entry positions including said virtual entry positions, col. 1, lines 58 – 67),

generating said validation information by combinatorial logic processing a process-related IN-pointer and OUT-pointer (e.g., Usually two pointers are provided, an in-pointer (103) and an out-pointer (104), which allow to run said circular buffer as a FIFO (first in first out) buffer. The in-pointer points to the first free entry position (107) of the circular buffer, which is adjacent to the buffer's most recently occupied entry. The in-pointer thus defines the head of the

stored entry sequence. Whenever a new entry is to be written to the buffer, it is placed at the entry position specified by the in-pointer. The in-pointer is then incremented, in order to again point to the next available entry position. The in-pointer thus defines the head of the entry sequence stored in the circular buffer, col. 2, lines 41 – 58),

for use in managing queues (e.g., This means that a new instruction from the instruction string is written to the first free entry of the instruction queue in the window buffer, col. 6, lines 44 – 46).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soell in view of Hilgendorf et. al. 5,930,491 (Hereafter Hilgendorf).

Soell does not specifically show the limitations of claims 4 and 9-11.

As per claim4, Hilgendorf teaches the following:

said buffer memory is a window buffer able to be filled with processing instructions, (e.g., As in conventional, sequential processing techniques, one starts with a stream of ordered instructions (100). These instructions (101) can either be of the RISC (Reduced Instruction Set Computing) type or of the CISC (Complex Instruction Set Computing) type. The S/390

instructions which IBM mainframes can process are of the CISC-type and also include instructions written in microcode, col. 4, lines 50 –56),

said processes being at least two of dispatching new instructions to said window buffer (e.g., Let's consider the case that both the internal IWB instructions 205 and 206 write their result to one certain target register, and that the internal instruction 207 uses the content of said register as source data. Therefore, instruction 207 can only be dispatched as soon as instruction 206 has been completed. Because of data dependencies, it is not possible to execute instructions 206 and 207 out of their regular order. From this example another feature of out-of-order processing systems becomes obvious: As both internal instructions 205 and 206 write to the same logical processor register, two physical instances of said logical register have to exist, col. 6, lines 45 – 60),

retiring instructions from said window buffer by a commit process (e.g., The same argumentation holds for the commit process. When committing instructions contained in different window buffers, the relative order of said instruction has to be taken care of (instructions have to be committed in sequential order). With the concept of a common instruction identifier a solution to this possible hazard can easily be found; an internal instruction in either window buffer must not be committed before all internal instructions with preceding instruction identifiers have been committed, col. 3, lines 32 – 40),

or purging at least one instruction from said window buffer (e.g., FIG. 5 shows how the range of instruction identifiers in use is modified when instructions are purged, fetched or committed, col. 4, lines 34 – 36),

a sub-unit for use in microprocessor devices having at least one storage device (e.g., FIG. 1 being split into an instruction window buffer (IWB) and a storage window buffer (SWB), col. 4, lines 21 – 23),

a microprocessor device having at least one sub-unit (e.g., an instruction can be forwarded from the reservation station to one of the processor's functional units, col. 1, lines 21 – 30),

a computer system having a microprocessor device (e.g., an instruction can be forwarded from the reservation station to one of the processor's functional units, col. 1, lines 21 – 30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Soell with the teachings of Hilgendorf in order to facilitate the instructions to be purged, fetched or committed for the instruction window buffer by the microprocessor.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haresh Patel whose telephone number is (703) 605-5234. The examiner can normally be reached on Monday, Tuesday, Thursday and Friday from 10:00 am to 8:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee, can be reached at (703) 305-8498.

The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) 306-5404.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Haresh Patel

October 10, 2003.

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100